REMARKS

This Amendment and Reply seeks to place this application in condition for allowance. The Specification has been amended to correct inadvertent typographical errors, improve grammar and/or clarity. The certain drawings have been corrected to more closely reflect the description of the invention(s) in the Specification. Moreover, several of the claims have been amended to correct inadvertent typographical errors, improve grammar, clarity and/or antecedent basis, and to more fully protect the Applicants' invention(s). No new matter has been added.

OFFICE ACTION

In the Office Action of June 7, 2004 (hereinafter the "Office Action"), the Examiner objected to certain drawings and claims as well as rejected other claims as being indefinite and/or unpatentable under §102(b). Moreover, several of the claims were found to contain patentable subject matter.

All of the objections and rejections raised in the Office Action have been addressed herein. Each of the objections and rejections are addressed below in detail and in the order presented in the Office Action.

Objections to the Drawings

The Applicants present herewith drawing replacement sheets that incorporate, among other things, the corrections requested by the Examiner. (See page 2 of the Office Action. The Applicants have also amended the drawings to correlate the number identifiers in the text with the number identifiers in the drawings and, as such, the

drawings more closely reflect the description of the invention(s) in the Specification. No new matter has been added.

Notably, in accordance with Rule 1.121(d), the attached amended drawings include the requisite label "Replacement Sheet" in the header of each sheet.

Applicants respectfully request that these drawings be accepted.

Objections to the Claims

All of the objections raised in the Office Action have been addressed herein. The undersigned appreciates the thoroughness of the Examiner's review – as well as the time and effort therefor.

Claims Rejections – 35 USC § 112

Several of the claims were rejected as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention. Each of the rejections is addressed separately below.

Claims 33 and 34-36: Claim 33, after amendment, is dependent on claim 28; thereby addressing the rejection.

Claims 43 and 44-46: Claim 43, after amendment, is dependent on claim 39; thereby addressing the rejection.

Claim 50 (and claims 32, 33, 42, 43, 56 and 57): The "write control signal set" was intended to describe the one or more control signals provided by the control unit to the transistor to perform a write operation and/or store a data state in the memory cell. In order to address the Examiner's concerns, the claims have been

amended to recite "first write control signals" (claims 32, 42 and 56) or "second write control signals" (claims 33, 43 and 57). The first write control signals are control signals that are provided by the control unit to memory cell to store the first charge in the body region of the transistor. The second write control signals are the control signals provided by the control unit to store the second charge in the body region of the transistor by removing the charge through the source region of that transistor.

Finally, claim 50 was amended to recite the positive voltage that is applied to the drain; thereby addressing the rejection to claims 51-53 as well on the bases that claims 51-53 depended from claim 50.

Claim 51: Claim 51 was amended to correct the antecedent bases with respect to the "second positive voltage. The "first positive voltage" is first introduced in claim 50; claim 51 depends from claim 50. As such, it is believed that the antecedent bases issues have been corrected via the amendment to the claims.

The Examiner has also raised a concern regarding the existence of an embodiment with the first and second positive voltages.[1] Applicants, in connection with FIGURES 1-3, describe many different and inventive write control operations between pages 12 and 14. In one embodiment, a positive voltage pulse may be applied to the drain 22 and the gate 28 and majority carriers (in this embodiment, holes) are removed from the body 20 to the source 18. (See, the Specification, page 14, lines 10-12).

[1] Claims 50 and 51 are directed to providing and/or storing a second charge in the body of the transistor of the first memory cell. In this regard, applying a first positive voltage to the drain region of the transistor provides the second charge in the body. (See, Claim 50). The second charge may be stored in the body region of the transistor in response to removing the first positive voltage from the drain region of the transistor before removing a second positive voltage from the gate of the transistor. (See, Claim 51).

Claims 57 and 58-60: Claim 57, after amendment, is dependent on claim 47; thereby addressing the rejection.

Rejection of the Claims under 35 USC §§ 102 and 103

In the Office Action, many of the claims were rejected as being anticipated by Hamano et al. (U.S. Patent 4,298,962, hereinafter "Hamano"). Applicants respectfully disagree. For at least the reasons set forth below, none of the claims are anticipated by Hamano.

Hamano

Hamano describes a semiconductor memory cell 201 (disposed on substrate 202) including a transistor having a source 203 and a drain region 204, and depletion regions 211 and 212, respectively, extending therefrom.[2] The Hamano memory cell is capable of storing two data states. (See, Hamano, Col. 8, line 36 to Col. 9, line 50). In the Hamano transistor, "when a backward voltage is applied between the source 203 and drain 204 and the substrate 202 or when they are held at an equal potential, that is, a forward voltage is not applied between them, the depletion layers 211 and 212 are extended from the source 203 and 204 so that they can be connected at a position under the insulating film 205." (Hamano, Col. 7, lines 54-60). According to Hamano, in this way, the state of the majority carriers in the channel region 209 can be retained. (Hamano, Col. 7, lines 61-62).

[2] Hamano appears to describe two embodiments of semiconductor memory cells. (see, for example, Hamano Col. 7, lines 25-32). A first embodiment is described at Col. 3, line 53 to Col. 7, line 32 and Figures 1-5F. A second embodiment is described at Col. 7, line 33 to Col. 10, line 44 and Figures 6-11D. The Examiner appears to have focused exclusively on the second embodiment of Hamano. For the sake of brevity as well as responsiveness, these remarks focus on the same embodiment.

In operation, Hamano writes one of the two data states in the transistor 201 by applying a negative voltage to the gate 208' of the transistor 201. In response, "the depletion layer 211' extending from the source 203' and the depletion layer 212' extending from the drain 204' shrink, so that the isolation between the channel region 209' and substrate 202' is removed. Then, by the effect of the negative potential at the gate 208', positive holes 220 in the substrate 202' are accumulated in the channel region 209' ...." (Hamano, Col. 8, lines 39-46; see also, Figure 9A).

Hamano writes the second data state by applying a positive voltage to the gate of the transistor 201 – which "depletes the majority carrier in the channel region 209'" (Hamano, Col. 9, line 14-19). " ... the depletion layers 211' and 212' shrink, so that the channel region 209' is coupled to the substrate 202'. Because "the gate potential is a positive potential, the positive holes 220 in the channel region 209' are pushed back to the substrate 202' ...." (Hamano, Col. 9, lines 20-25; see also, Figure 9D). In this way, "the channel becomes in a depletion state of holes ...." (Hamano, Col. 9, lines 25-28).

Claimed Independent Inventions

For the sake of brevity, the discussion below focuses on only selected aspects or features of the independent claims. No inference or conclusion should be drawn therefrom.

Claim 28

Independent claim 28, as amended, describes a semiconductor memory array comprising a plurality of memory cells arranged in a matrix of rows and columns. The plurality of memory cells includes a first memory cell and a second memory cell, wherein the first and second memory cells each includes at least a

transistor to constitute the memory cell. The transistor includes a source region, a drain region, and a body region disposed between and adjacent to the source region and the drain region, wherein the body region is an electrically floating state. A gate is disposed over the body region.

Each memory cell includes at least two data states including (1) first data state representative of a first charge in the body region and (2) a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region.

Finally, claim 28 states the gate of the transistor of the first memory cell and the gate of the transistor of the second memory cell are connected.

Claim 37

Independent claim 37, as amended, describes, among other things, a semiconductor memory array including first and second memory cells. The memory cells each include a transistor to constitute the memory cell wherein the transistor includes a source region having impurities to provide a first conductivity type, a drain region having impurities to provide the first conductivity type, and a body region disposed between and adjacent to the source region and the drain region. The body region is electrically floating and includes impurities to provide a second conductivity type wherein the second conductivity type is different than the first conductivity type. A gate disposed over the body region.

The memory cells of claim 37 include (1) a first data state representative of a first charge in the body region wherein the first charge is substantially provided by impact

ionization, and (2) a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region.

Like claim 28, claim 37 states that the gate of the transistor of the first memory cell and the gate of the transistor of the second memory cell are connected.

Claim 47

Independent claim 47, as amended, describes a semiconductor memory array, disposed in or on a semiconductor layer which resides on or above an insulating layer of a substrate. The semiconductor memory array including first and second memory cells which each include a transistor to constitute the memory cell. Like claim 37, the transistor of claim 47 includes a source region having impurities to provide a first conductivity type, a drain region having impurities to provide the first conductivity type, and a body region disposed between and adjacent to the source and drain regions and the insulating layer of the substrate. The body region is electrically floating and includes impurities to provide a second conductivity type wherein the second conductivity type is different than the first conductivity type. A gate is spaced apart from, and capacitively coupled to, the body region.

The memory cells of claim 47 include (1) a first data state representative of a first charge in the body region, and (2) a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region. As with claims 28 and 37, claim 47 states that the gate of the transistor of the first memory cell and the gate of the transistor of the second memory cell are connected.

Hamano Does Not Anticipate the Claimed Independent Inventions

There are many inventions described in the instant application. In an effort to present a more concise response, the discussion below focuses on only selected aspects or features of the independent claims. These are not the only reasons the inventions of the independent claims are patentable over Hamano. As such, no inference or conclusion should be drawn that Applicants' response to this rejection is exhaustive; rather, for the sake of brevity, the remarks focus on only some of the patentable aspects or features of the independent claims.

Claim 28

Hamano does not teach or suggest, among other things, a memory cell constituted by a transistor that includes (1) a first data state representative of a first charge in the body region, and (2) a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region. Rather, Hamano forces the majority carriers from the channel region 209' to the substrate 202' by shrinking the depletion layers 211' and 212' so that the channel region 209' is coupled to the substrate 202'. (Hamano, Col. 9, lines 20-22 and Figure 9D). The holes 220 in Hamano are then pushed back into the substrate 202' as a result of a positive potential applied to the gate 208'. (See, Hamano, Col. 9, lines 23-25). Thus, Hamano describes a memory cell having a second data state that is created by forcing the majority carrier from the channel region 209' to the substrate 202'. The Hamano memory cell does not include a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body

region of the transistor (and the memory cell) through the source region of the transistor.[3]

Claim 37

Hamano does not teach or suggest, among other things, a memory cell constituted by a transistor that includes (1) a first data state representative of a first charge in the body region wherein the first charge is substantially provided by impact ionization, and (2) a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region. In short, the transistor of the Hamano memory neither provides a first charge in the body region substantially via impact ionization nor provides a second charge in the body region substantially via removing charge from the body region through the source region. Rather, Hamano, among other things, applies a negative potential to the gate 208' to cause positive holes 220 in the substrate 202' to accumulate in the channel region. (See, Hamano, Col. 8, lines 39-46; see also, Figure 9A). As such, Hamano does not provide a first charge in the body region which is substantially provided by impact ionization.

Moreover, as mentioned above, a data state is provided in the Hamano memory cell by forcing the majority carrier from the channel region 209' to the substrate 202'. That is, the holes 220 in Hamano are pushed back into the substrate 202' (via a positive voltage on the gate 208') after the shrinking the depletion layers 211' and 212'. (See,

[3] In first embodiment of Hamano, the majority carriers "flow out of the channel region 113 to the P-type region 105." (Hamano, Col. 4, lines 48-49). That is, the "holes are swept out through the P-type impurity region 105", so that the channel region takes a depletion state of majoiryt carriers ...." (Hamano, Col. 6, lines 55-59).

Hamano, Col. 9, lines 20-25; see also, Figure 9D). As such, Hamano does not include a second data state representative of a second charge in the body region wherein the second charge is substantially provided (by removing charge from the memory cell) by removing majority carriers from body region of the transistor through the source region.

Claim 47

Hamano does not teach or suggest, among other things, (i) a semiconductor memory array, disposed in or on a semiconductor layer which resides on or above an insulating layer of a substrate or (ii) a body region that is disposed between and adjacent to the source and drain regions and the insulating layer of the substrate. In addition, Hamano does not teach or suggest a memory cell constituted by a transistor that includes a first data state representative of a first charge in the body region, and a second data state representative of a second charge in the body region wherein the second charge is substantially provided by removing charge from the body region through the source region.

Hamano appears to be fabricated in or on a bulk-type semiconductor substrate – not in or on a semiconductor layer which resides on or above an insulating layer. (See, for example, Hamano, Col. 8, lines 33-35 and Col. 9, line 66 to Col. 10, line 44, and Figures 9A-9F and 11A-11D). As such, assuming for the sake of argument that Hamano includes a body region, that body region is not disposed between and adjacent to the source and drain regions and the insulating layer of the substrate.

In addition, as mentioned above, the Hamano memory does not provide a second charge in the body region substantially via removing charge from the body region through the source region. Rather, Hamano forces the majority carrier from the

channel region 209' to the substrate 202' by shrinking the depletion layers 211' and 212'. In this way, the majority carriers may move from the channel region 209' to the substrate 202' under the influence of a positive voltage applied to the gate 208', which pushes the holes 220' into the substrate 202'. (Hamano, Col. 9, lines 20-25; see also, Figure 9D).

Dependent Claims

Several of the dependent claims have already been found to include patentable subject matter. As for the rejected dependent claims, for the sake of brevity, the additional reasons/bases that those dependent claims are patentable over Hamano are not set forth herein. However, for at least the reasons stated above, it is respectfully submitted that such rejected dependent claims are patentable in view of Hamano.

Statement of Reasons for the Indication of Allowable Subject Matter

Several of the claims were found to contain patentable subject matter in the initial Action. No inference or conclusion should be drawn that Applicants believe that the Examiner's reasons for allowance are the only reasons those claims are patentable -- whether based on the subject matter of the dependent claim or a preceding claim(s). Indeed, it is the Applicants' position that such claims are also patentable for the same reasons expressed above.

Prior Art Made of Record

Applicants note the prior art made of record but not relied upon. It is not clear what is the relevance of (or meant by) the comment that the prior art made of record "is considered pertinent to applicant's disclosure." (See, Office Action, page 6,

paragraph 9). No inference or conclusion should be drawn that Applicants agree, in any way, with the Examiner's characterization of such prior art. In an effort to provide a more concise response, and because the Examiner has not rejected any of the claims based on the prior art made of record, Applicants provide no comment on the Examiner's characterization.

Amendment to the Claims

Several of the claims have been amended to correct inadvertent typographical errors, improve grammar, clarity and/or antecedent basis, and to more fully protect the Applicants' invention(s). No new matter has been added.

Notably, none of the amendments were motivated by patentability considerations in view of the prior art, including the art relied on in the outstanding Office Action.

CONCLUSION

Applicants respectfully request entry of the foregoing amendment and reconsideration of the instant application. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

It is noted that should a telephone interview expedite the prosecution of this application in any way, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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